Remarks

Specification correction

The correction to page 3 does not add new matter since the preceding sentence in the specification makes it clear that the source interconnects 310 and drain interconnects 312 are formed into comb-like structures.

Claim Rejections – 35 USC 102

Claims 1, 2 5-7 were rejected under 35 USC 102 over Donoghue.

As is discussed in greater detail below, Donoghue does not deal with a transistor configuration where multiple MOS devices are connected in parallel. This is not surprising since Donoghue is not trying to provide a high power arrangement. Instead it deals with a memory device and the orientation of reference cells (see title and first three lines of the abstract of Donoghue). Thus there is no need for current sharing between multiple MOS transistors, and Donoghue does not teach such current sharing.

In particular, with respect to claim 1, the sources and drains shown in Figure 8 of Donoghue are not connected in parallel. To be in parallel, the sources would have to be connected together, and the drains would have to be connected together as shown, for example, in Figure 2 of the present application.

Regarding claim 2, Figure 8 of Donghue shows adjacent transistors connected drain-to-source. No common drain or source interconnect is shown or described in Donoghue.

In contrast, the present application has its drains connected together by a common drain interconnect and its sources connected together by a common source interconnect as shown in Figure 2.

Regarding claim 5, this depends from claims 1 and 2 and therefore includes the limitations of claims 1 and 2.

Regarding claim 6, the drains and sources in Donoghue do not alternate but, nevertheless have multiple contacts 336, 338 for the drains and multiple contacts 324, 326 for the sources as

shown in Figure 3 of Donoghue. In contrast, Figure 3 and page 3, line 8-13 of the present application show and describe source regions 304 and drain regions 306 alternating on either side of the polygate 300 to provide a drain-source followed by a source-drain MOS. No such alternating drain-source configuration is shown in Figure 3 of Donoghue. In fact, Figure 3 of Donoghue shows sources 316, 318 lying next to each other. Similarly drains 328, 330 lie next to each other. Figure 8 of Donoghue also confirms that the MOS transistors are arranged drain-source, drain-source, and do not alternate.

Regarding claim 7, Donoghue does not show drain contacts on each side of the polygate, or source contacts on each side of the polygate. Structures 368-371 define the gates. As shown in Figure 3 of Donoghue, the drain contacts 336, 338, are both on one side of the gates. Similarly both source contacts 324, 326 are on one side of the gates, rather than being on both or each side of the gates.

In view of the explanation above, it is respectfully submitted that all of the claims are in a condition for allowance and early allowance is therefore requested.

Respectfully Submitted,

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